IN THE CLAIMS:

Cancel claim 4 and rewrite the pending claims as follows:

1. (Currently amended) A method for improving resolution of a current mode driver, where the current mode driver is operable to provide an output that falls within a predetermined range, the method comprising the steps of:

sensing at least one of a process condition, a voltage condition and a temperature condition with a PVT detector;

adjusting a full scale current of a DAC in accordance with an output of the PVT detector; and

setting a current control signal based on an output of the DAC, the current control signal being applied to the current mode driver to improve resolution of the current mode driver, wherein the current control signal for transistors in the current mode driver includes a plurality of bits.

2. (Previously presented) The method for improving resolution of a current mode driver as claimed in claim 1, wherein the step of adjusting the full scale current comprises the steps of:

generating an adjustment signal in response to the sensing step; and

applying the adjustment signal to the current mode driver, the adjustment signal causing the current mode driver to adjust the full scale current.

3. (Previously presented) The method as claimed in claim 2, wherein the step of applying the adjustment signal to the current mode driver comprises applying at least one predetermined voltage to a corresponding at least one transistor switch.

4. (Cancelled)

5. (Currently amended) The method as claimed in claim 1, wherein the sensing operation ~~step~~ comprises determining a timing condition associated with a phase-locked loop.

6. (Currently amended) The method as claimed in claim 1, wherein the sensing operation ~~step~~ comprises determining a timing condition associated with a delayed locked loop.

7. (Previously presented) The method as claimed in claim 1, wherein the sensing step comprises the steps of:

applying a PVT independent current to a PVT sensitive load; and

detecting a voltage drop across the PVT sensitive load.

8. (Previously presented) The method as claimed in claim 1, wherein the sensing step comprises the steps of:

applying a pulse in parallel to a delay line and a first plurality of latches, wherein the delay line comprises a second plurality of delay stages;

coupling an output of a subset of the plurality of delay stages to an input of a corresponding latch from the plurality of latches; and

decoding an output from the plurality of latches.

9. (Previously presented) The method as claimed in claim 1, wherein the sensing set comprises sensing a PVT sensitive DC parameter.

10. (Previously presented) The method as claimed in claim 1, wherein the sensing step comprises sensing a PVT sensitive AC parameter.

11. (Previously presented) In an output driver that is operable to provide a multi-PAM output having at least two levels, wherein the output is set in accordance with a current control signal, a method of improving resolution of the output driver, the method comprising the steps of:

applying the current control signal to cause the output driver to sink a full scale current;

providing a PVT detector to sense a characteristic that comprises at least one of a process condition, a voltage condition and a temperature condition;

generating a full scale current adjustment signal at the PVT detector;

applying a full scale current adjustment signal to alter the full scale current of the output driver;

applying the current control signal to cause the output driver to sink a second current, wherein the second current is less than the full scale current;

sensing, at the PVT detector, at least one of a process condition, a voltage condition and a temperature condition;

generating a second current adjustment signal at the PVT detector;

applying the second current adjustment signal to alter the second current of the output driver; and

calibrating the altered full scale current of the output driver and the altered second current of the output driver by comparing the altered full scale current with a first reference and comparing the altered second current with a second reference.

12. (Previously presented) The method of improving resolution of an output driver as claimed in claim 11, wherein the step of applying the full scale current adjustment signal comprises coupling the adjustment signal to a digital-to-analog converter.

13. (Previously presented) The method of improving resolution of an output driver as claimed in claim 12, wherein the adjustment signal is a two-bit signal and the digital-to-analog converter has at least two inputs.

14. (Previously presented) The method of improving resolution of an output driver as claimed in claim 12, wherein the digital-to-analog converter provides an output signal in response to the adjustment signal.

15. (Previously presented) A method of improving resolution of a current mode driver, comprising the steps of:

applying a first current control signal to a digital-to-analog converter, the digital-to-analog converter providing a first output in response thereto;

applying the first output as a gate voltage to control a full scale current of an output driver;

calibrating the output driver by comparing a second output, which is provided by the output driver, with a reference; and

augmenting the first current control signal when the second output differs from the reference.

16. (Previously presented) The method as claimed in claim 15, wherein the step of calibrating the output driver comprises deriving the second output from a signal provided directly to the output driver.

17. (Previously presented) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a resistive divider.

18. (Previously presented) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a transconductance stage.

19. (Previously presented) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a switched capacitor circuit.

20. (Previously presented) The method as claimed in claim 15, wherein the first current control signal is applied under user control.

21. (Currently amended) The method of claim 1, wherein the current mode driver is a multi-PAM signal generator coupled to a bus, the multi-PAM signal generator uses pulses having a plurality of sets of signal amplitudes to encode signals, and wherein a respective set of signal amplitudes in the plurality of sets of signal amplitudes has at least two signal levels.

22. (Previously presented) The method of claim 21, wherein the sensing, adjusting and setting steps occur during a power-up sequence for the multi-PAM signal generator.

23. (Previously presented) The method of claim 21, wherein the adjusting and setting steps occur in response to a triggering event after power-up.